5442-025 SCM

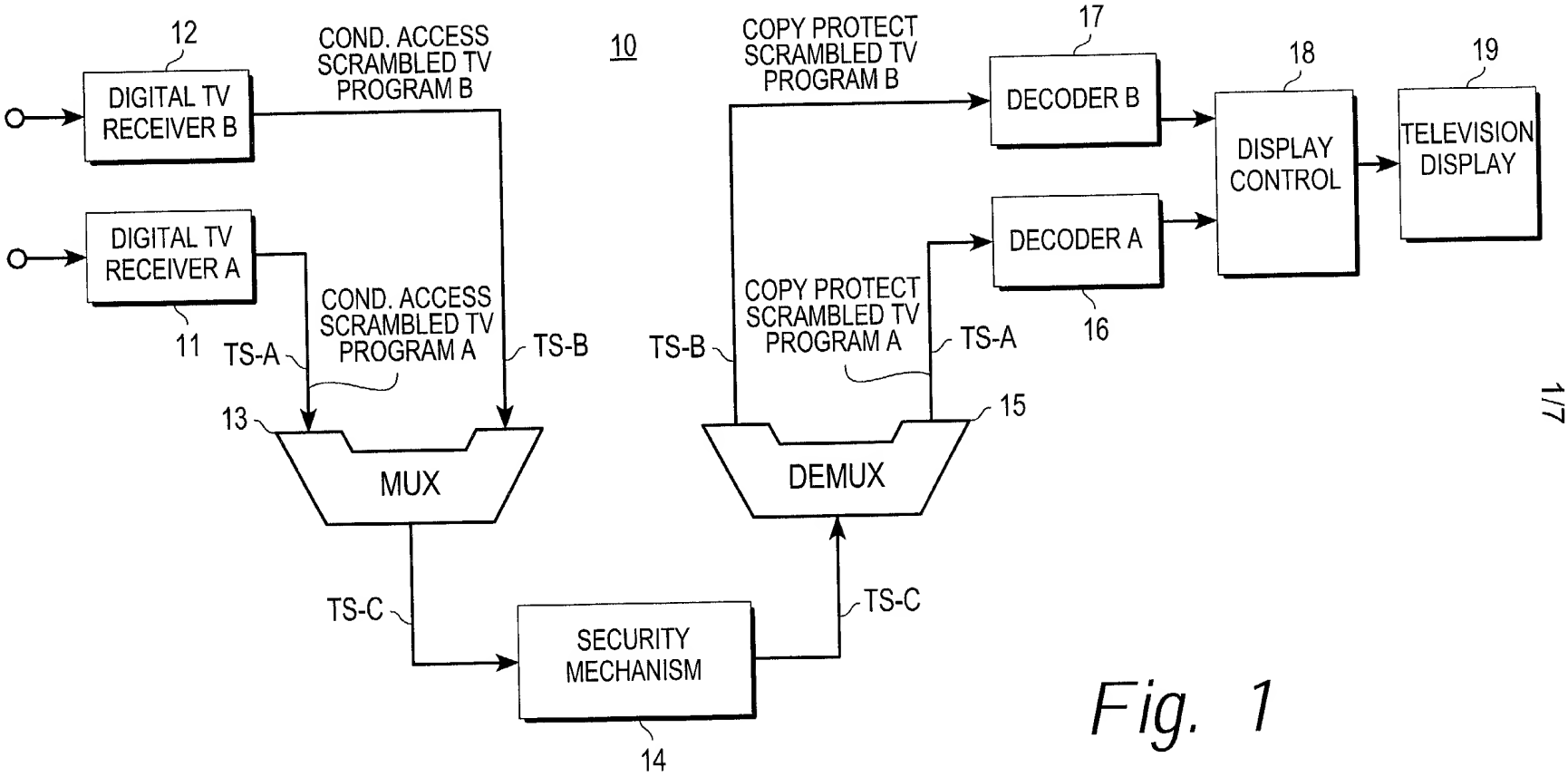

Fig. 1

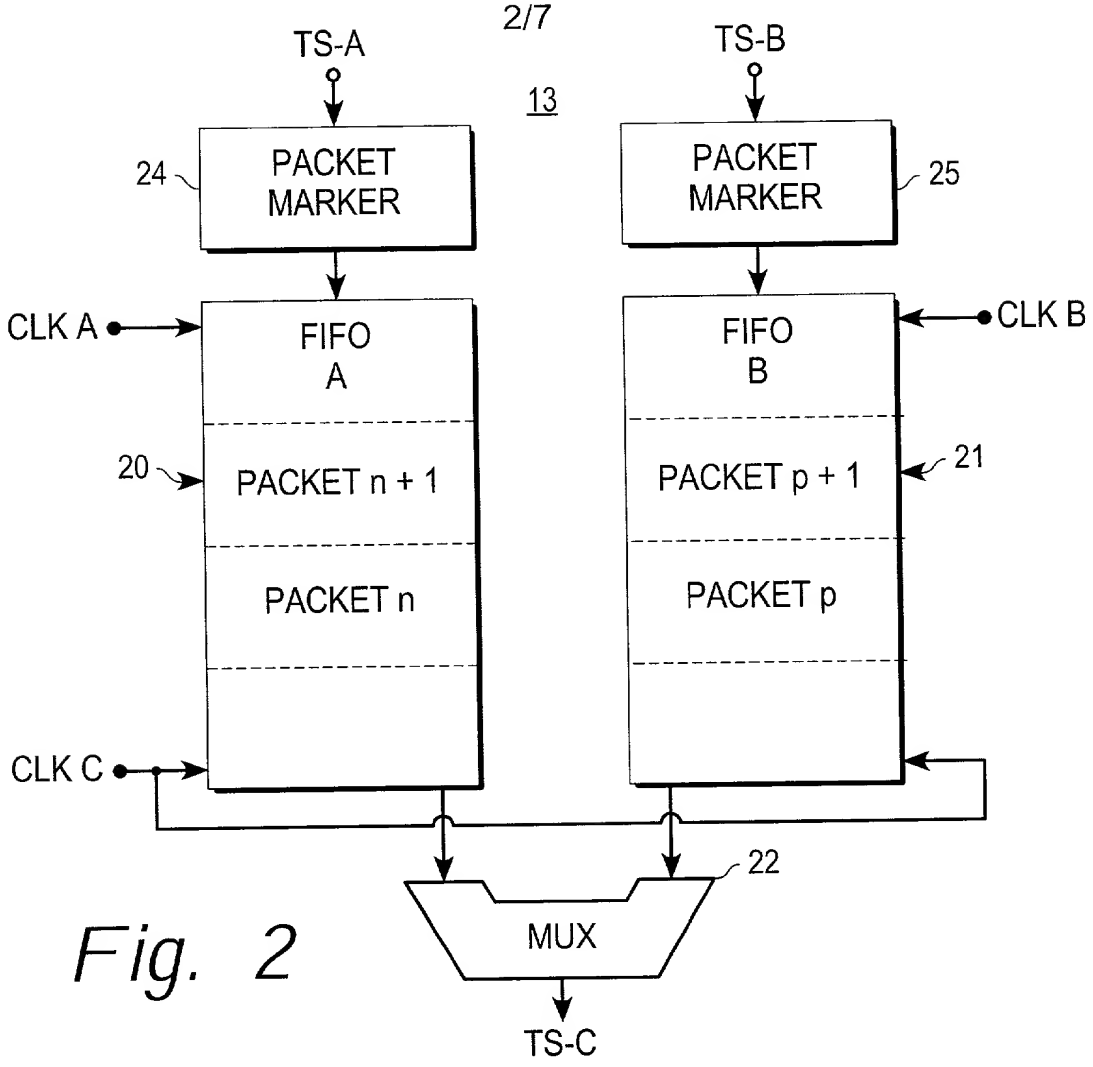
TS-A
TS-B
13
24
PACKET MARKER
25
PACKET MARKER
CLK A
FIFO A
FIFO B
CLK B
20
PACKET n + 1
21
PACKET p + 1
PACKET n
PACKET p
CLK C
22
MUX
TS-C

Fig. 2

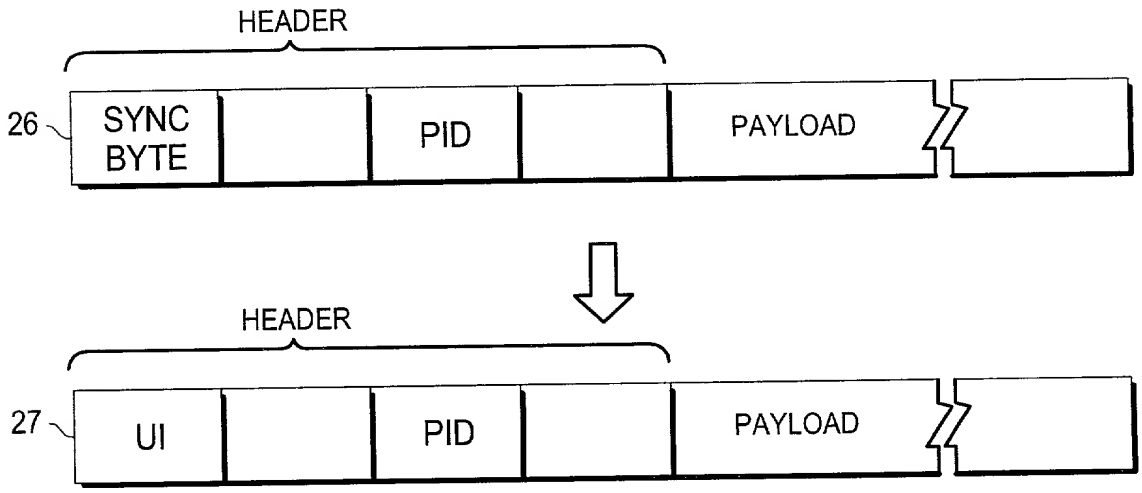
HEADER
26
SYNC BYTE
PID
PAYLOAD
HEADER
27
UI
PID
PAYLOAD

Fig. 3

CHANNEL	UI
RECEIVER A	0x47
RECEIVER B	0x46
RECEIVER C	0x45
RECEIVER D	0x44
RECEIVER E	0x43
RECEIVER F	0x42
RECEIVER G	0x41
RECEIVER H	0x40

Fig. 4

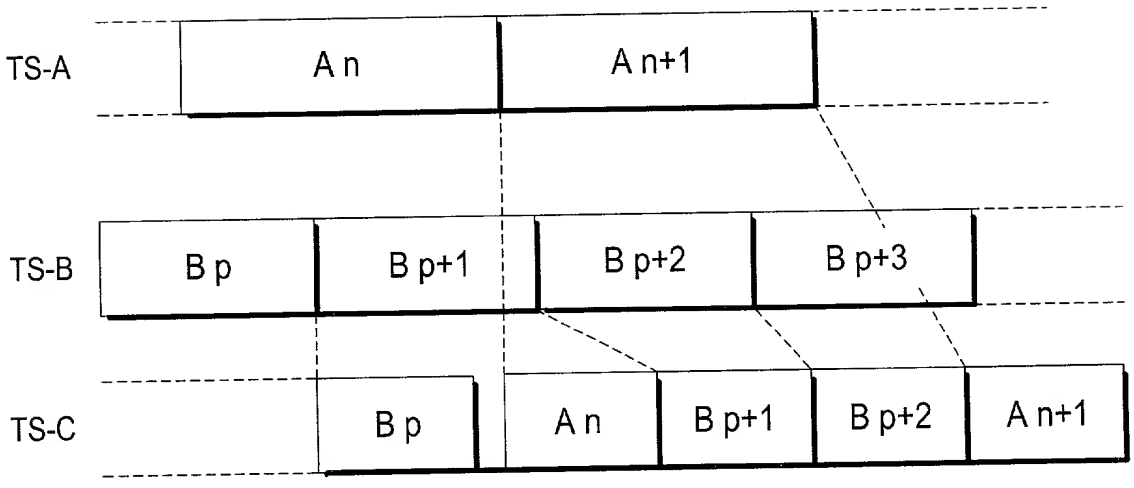

Fig. 5

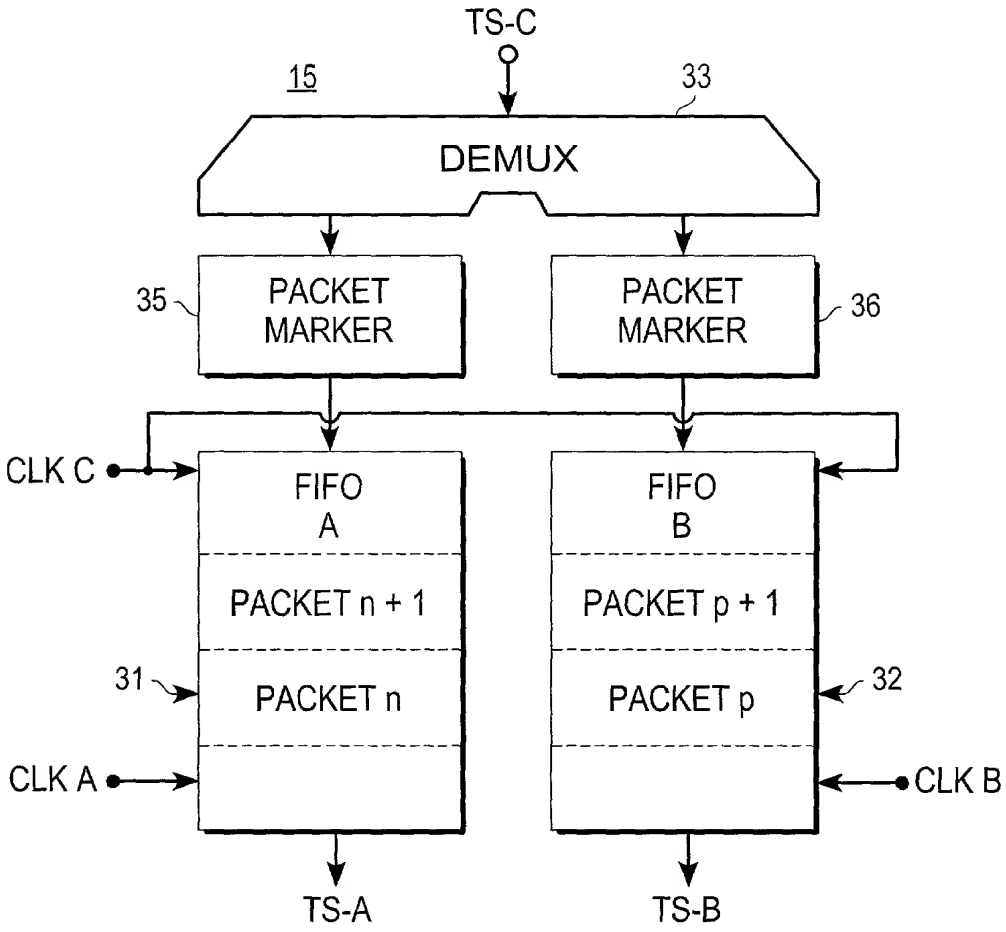
TS-C
15
33
DEMUX
35
PACKET MARKER
PACKET MARKER
36
CLK C
FIFO A
FIFO B
PACKET n + 1
PACKET p + 1
31
PACKET n
PACKET p
32
CLK A
CLK B
TS-A
TS-B

Fig. 6

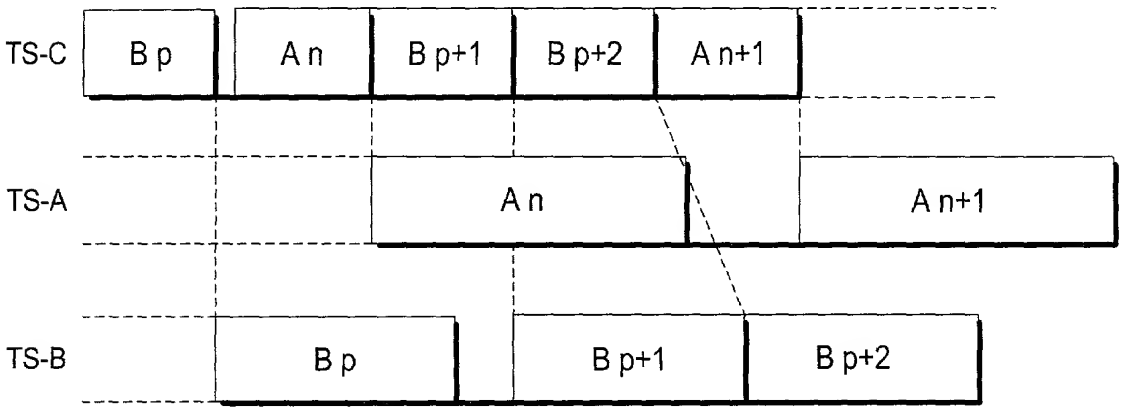
TS-C
B p
A n
B p+1
B p+2
A n+1
TS-A
A n
A n+1
TS-B
B p
B p+1
B p+2

Fig. 7

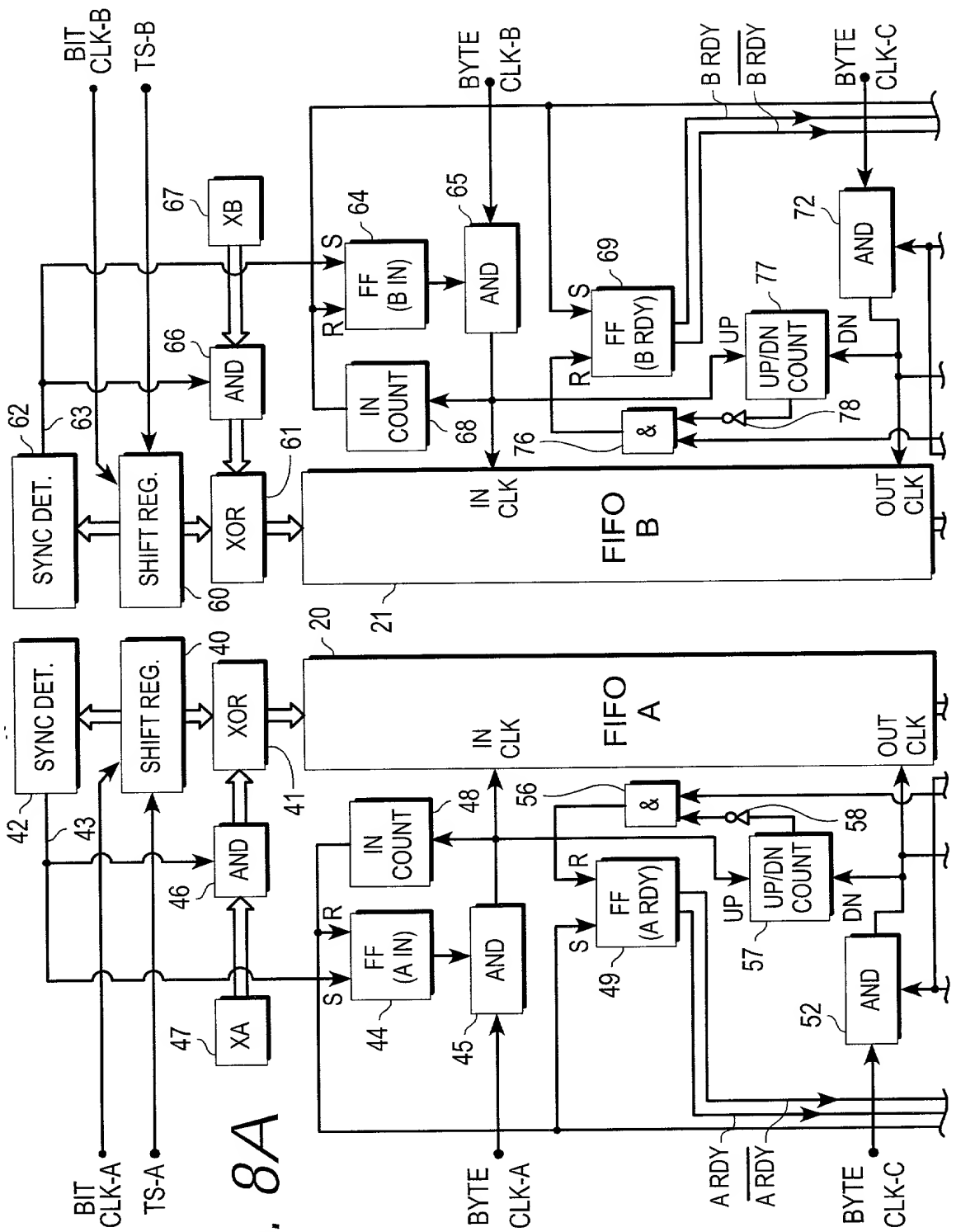
BIT CLK-A
TS-A
BIT CLK-B
TS-B
SYNC DET.
SHIFT REG.
XOR
AND
XA
XB
FF (A IN)
FF (B IN)
IN COUNT
FF (A RDY)
FF (B RDY)
UP/DN COUNT
&
FIFO A
FIFO B
IN CLK
OUT CLK
BYTE CLK-A
BYTE CLK-B
BYTE CLK-C
A RDY
B RDY
UP
DN
R
S

Fig. 8A

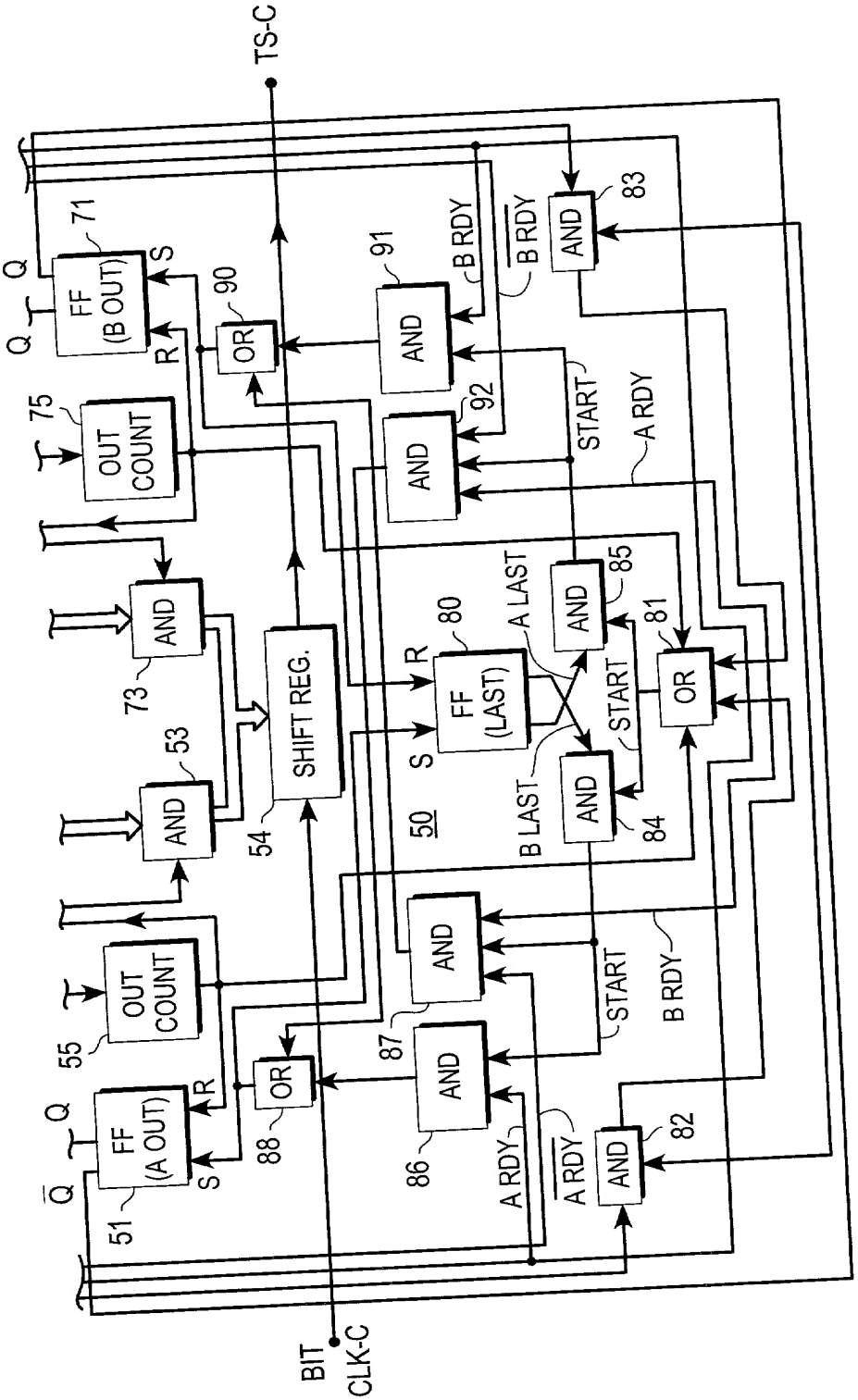
TS-C
BIT CLK-C
FF (A OUT)
FF (B OUT)
FF (LAST)
OUT COUNT
OUT COUNT
SHIFT REG.
AND
OR
A RDY
B RDY
START
A LAST
B LAST
50
51
53
54
55
71
73
75
80
81
82
83
84
85
86
87
88
90
91
92

Fig. 8B

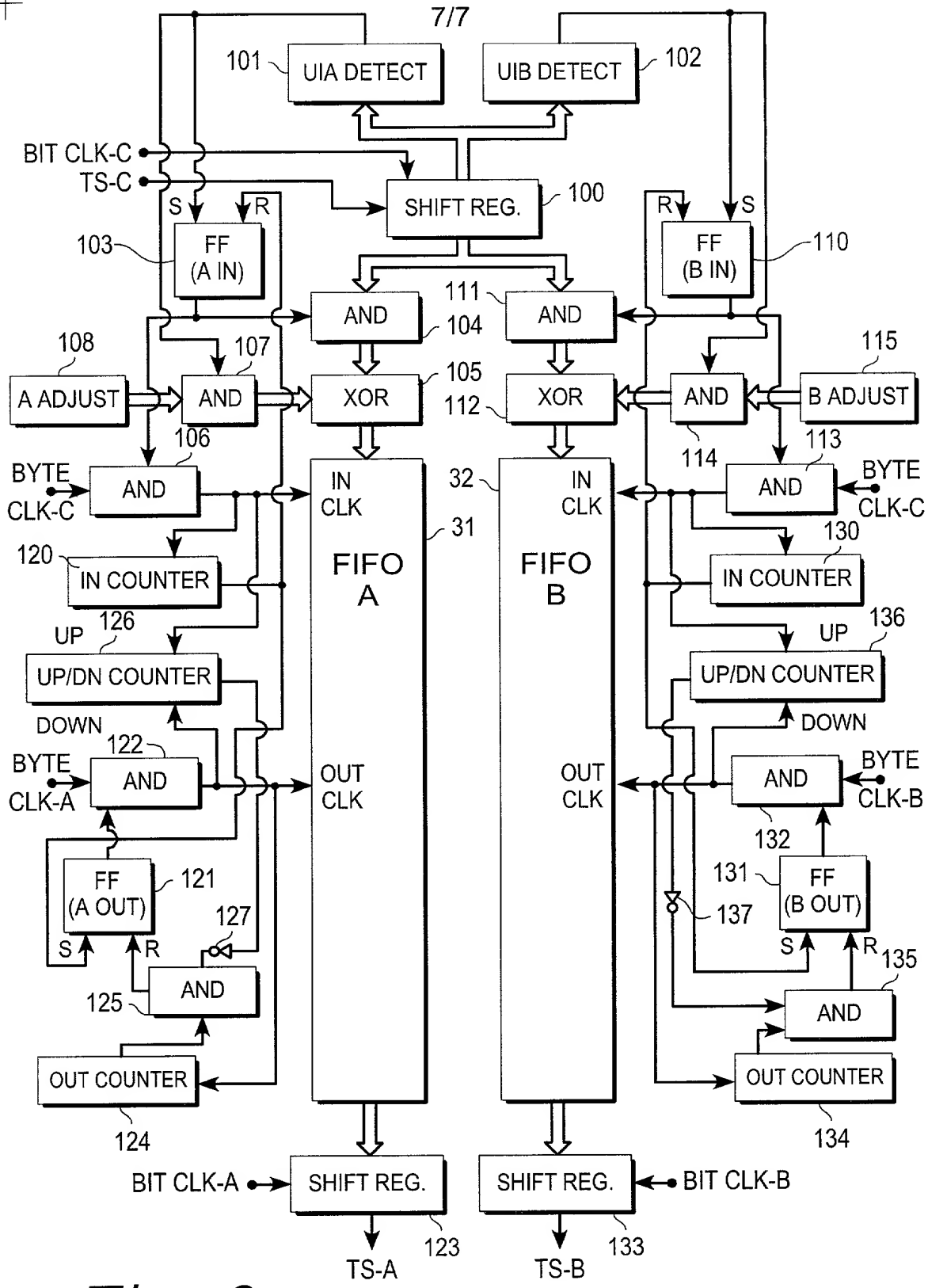
101
UIA DETECT
UIB DETECT
102
BIT CLK-C
TS-C
SHIFT REG.
100
S
R
R
S
103
FF
(A IN)
FF
(B IN)
110
111
AND
AND
104
108
107
115
A ADJUST
AND
XOR
105
XOR
112
AND
B ADJUST
106
114
113
BYTE
CLK-C
AND
IN
CLK
32
IN
CLK
AND
BYTE
CLK-C
31
FIFO
A
FIFO
B
120
IN COUNTER
130
IN COUNTER
126
UP
UP
136
UP/DN COUNTER
UP/DN COUNTER
DOWN
DOWN
122
BYTE
CLK-A
AND
OUT
CLK
OUT
CLK
AND
BYTE
CLK-B
132
131
FF
(A OUT)
121
137
FF
(B OUT)
127
S
R
S
R
135
AND
125
AND
OUT COUNTER
OUT COUNTER
124
134
BIT CLK-A
SHIFT REG.
SHIFT REG.
BIT CLK-B
123
133
TS-A
TS-B

Fig. 9